A Reduced Power Switches Count Multilevel Converter-Based Photovoltaic System with Integrated Energy Storage

Lashab, Abderezak; Séra, Dezso; Hahn, Frederik; Camurca, Luis; Liserre, Marco; Guerrero, Josep M.

Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2020.3009594

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

A Reduced Power Switches Count Multilevel Converter-Based Photovoltaic System with Integrated Energy Storage

Abderezak Lashab, *Student Member, IEEE,* Dezso Sera, *Senior Member, IEEE,* Frederik Hahn, *Student Member, IEEE*, Luis Camurca, *Student Member, IEEE,* Marco Liserre, *Fellow, IEEE,* and Josep M. Guerrero, *Fellow, IEEE*

***Abstract*—A multilevel topology for photovoltaic (PV) systems with integrated energy storage (ES) is presented in this paper. Both PV and ES power cells are connected in series to form a DC-link, which is then connected to an H-bridge to convert the DC voltage to an AC one. The main advantage of the proposed converter compared to the cascaded-H-bridge (CHB) converter, as well as compared to the available multilevel topologies, is that fewer semiconductor devices are needed here. As the output voltage levels increase, more switches are saved, which results in a more efficient, cheaper, and smaller converter. So far, there is still no modulation strategy that is designed particularly for PV-fed multilevel converters with built-in ES. The standard modulations are unpractical for such an application since they suffer from deficiencies such as polluted output signals—thus, requiring larger output-filter—and over-modulation. A modified modulation strategy for PV+ES multilevel inverters is, therefore, introduced in this work. The proposal has been simulated and experimentally validated to evaluate its effectiveness, where it has been shown that the proposed topology is not exclusively feasible, but also suffers from less conduction and switching loss, achieving higher efficiency with respect to its counterpart the CHB.**

I. Introduction

GIVEN the cost, power loss, size, and weight associated with the switching harmonics filter and transformer of two-level inverters, manufacturers are investigating multilevel ones for the feasibility of direct connection, converter to AC medium-voltage [1]-[2]. Moreover, the solar power harvesting increases by installing PV arrays in each cell, separately, and operate each one at its maximum power [3]. The literature survey shows that in multilevel converters category, several types have been proposed for PV power applications, such as, modular multilevel converter (MMC) [4], CHB [5], cascaded Z-source [6], cascaded quasi Z-source (qZS) [7], and multilevel DC-link (M-DC-link) [8]-[9].

In the recent years, PV systems are involved as a major part of renewable energy resources in both micro-grid and large power system applications. Nevertheless, as the load demand does not meet the solar production in all the times, a means that stores the energy for non-solar covered periods is indispensable for an uninterruptible power supply [10]. In addition, PV systems with integrated ES can provide ancillary services to the grid operators such as, voltage support and frequency regulation [11]. The CHB topology for PV systems with ES is presented in [12] and [13], where the PV modules are feeding some power cells, while the ES are connected to other cells (see Fig. 1(a)). The configuration in these two references is similar, except that in the former the ES system is battery-based, while in the last super-capacitor is the storage element. In [14], each cell of CHB is fed by PV panels and batteries, where the PV panels are connected to the DC-links through boost converters, while the batteries are interfaced by bidirectional-boost converters (this topology is referred to as CHBB thereafter). Due to the separate control of the maximum power point trackers (MPPT) and state-of-charge (SOC) of the batteries through the two employed boost converters, the control is simple and the configuration is flexible; however, a high number of power switches and passives is used. A cell with a small battery is added into a PV-fed CHB configuration in [15], where the aim is to mitigate the high-order harmonics caused by the partial shading among the cells. The PV-fed CHB with integrated ES has been used differently in [16], where the ES is connected in series to the line through an AC voltage regulator. In [17], an MMC for PV systems with integrated ES has been proposed, where the PV panels are feeding each cell separately, whereas the batteries are installed on the DC side of the MMC. Nevertheless, the batteries being on the DC side of the MMC seems inconvenient, due to the batteries low voltage nature. In [18], a battery has been integrated into qZS inverter, by connecting it in parallel with the first qZS capacitor C_1, while the authors in [19] proposed installing it in parallel with the second qZS capacitor C_2, instead. The second configuration seems to be more advantageous due to the lower voltage ratings of the second qZS capacitor C_2. This configuration has been extended for a multilevel one in [20], where a detailed controller parameters design is also provided.

Manuscript received August 17, 2019; revised April 28, 2020; accepted July 02, 2020. The work of J. M. Guerrero was funded by a Villum Investigator under Grant no. 25920 from The Villum Fonden. (*Corresponding author: Abderezak Lashab.*)

A. Lashab, D. Sera, J. M. Guerrero are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: abl@et.aau.dk; des@et.aau.dk; Joz@et.aau.dk).

F. Hahn, L. Camurca, and M. Liserre are with the Chair of Power Electronics, Kiel University, 24143 Kiel, Germany (e-mail: frha@tf.uni-kiel.de; lc@tf.uni-kiel.de; ml@tf.uni-kiel.de).

In this paper, a M-DC-link converter is proposed, where the DC-link is formed with a series connection of PV and battery cells. The proposed topology uses almost 50% fewer switches compared to the CHB which significantly reduces the loss and price of the converter. It has to be noted that, this paper is an extension of [21], where the idea was first introduced.

In some CHB's cases, such as in [22]-[23], dealing with different power levels among the cells without affecting the current injected to the grid is straightforward; however, at the expense of output filter in each cell, which makes the advantage of using a small filter in multilevel converters lost. Consequently, the power loss and price of the converter are higher. Besides, the PV cells may enter the over-modulation region under high solar irradiance levels if the PV arrays are not uniformly segmented and/or the ES cells are not charged in a proper manner. In [24], a remedy to the over-modulation issue has been proposed; however, the concept is to deliberately make the PV arrays operate under higher voltages away from their MPP points, which affects the system's overall efficiency negatively. To evade the aforementioned provisions, a modulation stage, which is from the phase-shifted pulse-width-modulation (PS-PWM) family, has been designed in this paper, accordingly.

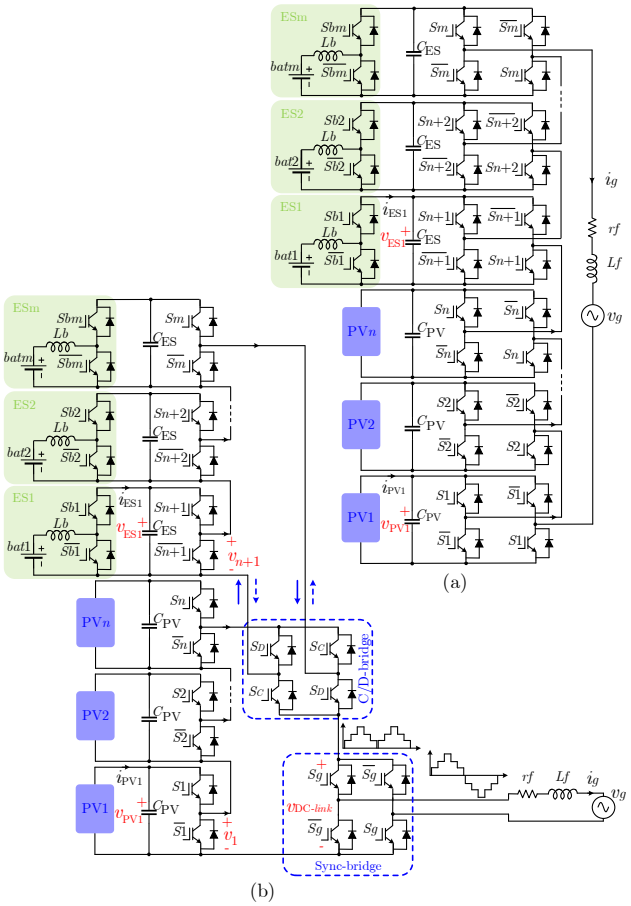

Fig. 1. (a) The conventional CHB and (b) proposed M-DC-link topology for PV systems with built-in ES.

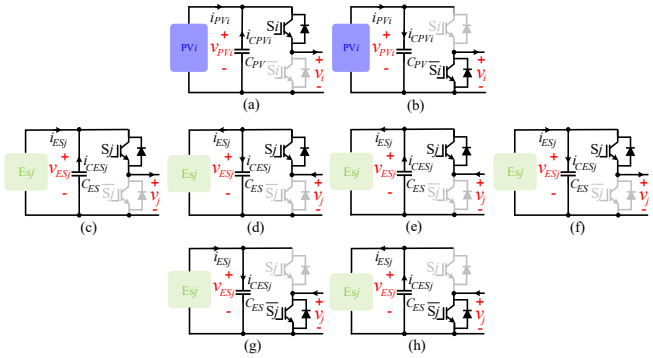

Fig. 2. Operation states in the PV and ES power cells.

II. Circuit Configuration of the PV-fed Multilevel DC-Link Converter with Integrated ES

The proposed PV-fed multilevel grid-connected converter with integrated ES is shown in Fig. 1(b). The number of PV cells is n, while that of the ES is m-n. The literature survey shows that, the PV cells count is higher in some configurations, such as in [12]-[13], while it is the other way around in other configurations [25]. Accordingly, although either case can be considered for the proposed converter, it is assumed that the total cells count is equivalently divided between the PV and ES ones. All the cells are half-bridge type, where the PV panels are connected directly, while the batteries are interfaced by bidirectional-boost converters. Similar to the conventional CHB, Sx and $\overline{Sx}$ in Fig. 1(b) are a complimentary pair of switches, where x is $i\in[1,n]$ and $j\in[n+1,m]$. The PV cells are connected in series, and are serially connected to the ES ones through an H-bridge (thereafter referred to as C/D-bridge), where the aim of using this later is to invert the voltage in the ES cells for both charging and discharging modes. Consequently, Sc and SD in the C/D-bridge are gated for charging and discharging modes, respectively. The sum of all these cells is inverted synchronously with the grid through a low frequency H-bridge (thereafter referred to as Sync-bridge). The topology can be extended for a three-phase equivalent by adding two similar parts for the remaining phases.

III. Analysis of the PV-Fed Multilevel DC-Link Converter with Integrated ES

A. Cells mathematical model

Each PV cell produces the voltages of either $v_{\mathrm{PV}i}$ or 0 to the DC-link, while the ES ones produce either $v_{\mathrm{ES}j}$ or 0. Where $v_{\mathrm{PV}i}$ and $v_{\mathrm{ES}j}$ are the voltages in the ith PV cell and jth ES cell, respectively. The ES cells can be inverted to $-v_{\mathrm{ES}i}$ through the C/D-bridge, as shown in Fig. 1(b).

The ith PV cell is inserted when the switch S_i is ON, as shown in Fig. 2(a). During this state, it is then dynamically characterized as,

$$\Delta v_{\mathrm{PV}i} = \frac{1}{C_{\mathrm{PV}}} \int \left(i_{\mathrm{PV}i} - \left\| i_g \right\| \right) dt \qquad (1)$$

such as, $i_{\mathrm{PV}i}$ is the ith PV array current, i_g is the current injected to the grid, and C_{PV} is the capacitor in each PV cell.

When the PV cell is bypassed as shown in Fig. 2(b), its dynamics are restricted to its local parameters as,

$$\Delta v_{\mathrm{PV}i} = \frac{1}{C_{\mathrm{PV}}} \int i_{\mathrm{PV}i}\, dt. \tag{2}$$

As it can be seen from Fig. 2(c) and (d), for the cases when both the ES cell capacitor (C_{ES}) and battery are in discharging mode or both are in charging mode, and when the cell is inserted, the cell dynamic characteristic can be written as,

$$\Delta v_{\mathrm{ES}j} = \frac{1}{C_{\mathrm{ES}}} \int \left(\gamma \left\| i_g \right\| - i_{\mathrm{ES}j} \right) dt \tag{3}$$

where, $i_{\mathrm{ES}j}$ is the current going into the jth ES cell, and γ is the C/D-bridge state, which takes the value of positive one, negative one, and zero during, respectively, discharging, charging, and float modes. Whereas, as shown in Fig. 2(e) and (g), in case of either the battery or the capacitor are in discharging mode, and when the cell is inserted,

$$\Delta v_{\mathrm{ES}j} = \frac{1}{C_{\mathrm{ES}}} \int \left(i_{\mathrm{ES}j} - \gamma \left\| i_g \right\| \right) dt. \tag{4}$$

As illustrated by Fig. 2(g), in case the ES cell is bypassed and the battery is discharging, the capacitor C_{ES} charges as,

$$\Delta v_{\mathrm{ES}j} = \frac{1}{C_{\mathrm{ES}}} \int i_{\mathrm{ES}j}\, dt. \tag{5}$$

Whereas in case the ES cell is bypassed and the battery is charging (Fig. 2(h)), the capacitor C_{ES} discharges as,

$$\Delta v_{\mathrm{ES}j} = -\frac{1}{C_{\mathrm{ES}}} \int i_{\mathrm{ES}j}\, dt. \tag{6}$$

B. Operation modes

1) During high irradiance levels

During high irradiance levels, and when the power generated by the PV strings is larger than the power required by the grid, the PV cells inject the harvested power into the grid, and the surplus of it is used to charge the batteries. The C/D-bridge, in this case, is set to charging mode. The power exchanged by the ES, in this case, is determined as follows,

$$P_{\mathrm{ES}} = P^{ref} - P_{\mathrm{PV}} \tag{7}$$

where P_{ES}, P^{ref}, and P_{PV} are the power exchanged by the ES cells, the grid active power reference, and the power generated by the PV arrays. The default current exchanged by each battery is defined based on (7),

$$I_{\mathrm{ES}} = \frac{P_{\mathrm{ES}}}{(m-n)\, v_{\mathrm{ES}}} \tag{8}$$

From which, the effective current exchanged by each battery is estimated as,

$$i_{\mathrm{ES}j} = I_{\mathrm{ES}}\, \beta_j \tag{9}$$

where β_j is provided by the energy management system (EMS), which considers, among other things, the batteries' SOC balance, their cycles balance, as well as their safe operating regions. The EMS is developed such that the partial shading among the PV cells is also taken into account.

2) During low irradiance levels,

During low solar irradiance levels, when the power harvested by the PV panels is less than the one required by the grid, all the cells of both PV panels and batteries contribute to inject the required power to the grid. Thus, the C/D-bridge is set to discharging mode.

3) During irradiance levels equal to the power reference

When the power generated by the PV arrays is just equal to the power required by the grid, two choices are offered, such as injecting all the PV power to the grid and floating the batteries, or charging the batteries while injecting less power to the grid. The choice is made based on the highest price revenue to the plant owner, that is assumed in what follows to inject the power to the grid as inquired by its operator.

Accordingly, for all three mentioned modes, the governed grid voltage relationship with the filter parameters, as well as power cell voltages, takes the following form,

$$v_g = (2S_g - 1)\left(\sum_{i=1}^{n} v_{\mathrm{PV}i}\, S_i + \gamma \sum_{j=n+1}^{m} v_{\mathrm{ES}j}\, S_j \right) - r_f\, i_g - L_f \frac{di_g}{dt}. \tag{10}$$

where v_g is the grid voltage, L_f is the inductor of the output filter, r_f is the stray resistance of the filter, and S_g is the Sync-bridge switching signal.

C. Modified Modulation

During high irradiance levels, when the power generated by the PV cell is higher than the one inquired by the grid operator, the PV cell switching function (U_i^{ref}) is larger than the switching function required to inject the active power to the grid (U_P^{ref}), as illustrated in Fig. 3(a). Consequently, the PV gating pulse S_i is larger than the gating pulse matching the active power reference (S_P). The ES cell is, therefore, inserted at the same time the PV one is inserted, but at the two extreme edges of the PV gating pulse, enough to curtail the surplus of power, as indicated by the green color in Fig. 3(a). This mode of operation is executed solely when the battery's SOC is below the maximum one (SOC_{max}), otherwise, the PV cell operating point should be moved away from the MPP one.

When the PV cell is subjected to low solar irradiance levels that are insufficient to provide the required power to the grid, and the battery's SOC is above the minimum one (SOC_{min}), then the ES cell is inserted at the boundaries where the PV one

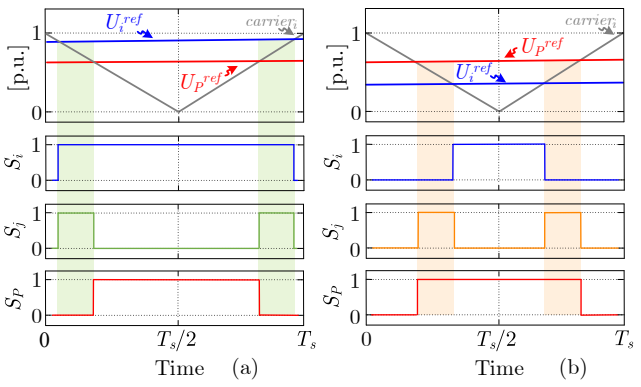

Fig. 3. The modified PS-PWM for the proposed M-DC-link converter during, (a) charging mode, and (b) discharging mode.

TABLE I.
COMPARISON OF THE PORPOSED TOPOLOGY WITH SOME OF THE EXISTING TOPOLOGIES

	CHB [12]	CHBB [14]		Proposed topology		
		Boost stage	H-bridge	Cells (PV&ES)	C/D-bridge	Sync-bridge
Switching frequency	f_s	$>f_s$ ×	f_s	f_s	$<<f_g$ ✓	f_g ✓
Current ratings	$i_{DCg}+I_g$ [ii]	$i_{PV}+0.5\Delta i_{PV}$	$i_{DCg}+I_g$	$i_{DCg}+I_g$	$i_{DCg}+I_g$	$i_{DCg}+I_g$
Voltage ratings	v_{cell} [i]	v_{cell}		v_{cell}	$v_{cell}\times n$ ×	$v_{cell}\times n$ ×
Voltage stress	dv_{cell}/dt	dv_{cell}/dt			dv_{cell}/dt	
Number of switches	$n\times 8$ ×	$n\times 6$ ×			$n\times 2+8$ ✓	
Inductors	- ✓	n ×			- ✓	
Dead-band between the gate drive signals	Necessary	Necessary		Necessary	Necessary	Not Necessary ✓

[i] v_{cell} is the nominal voltage in both PV and ES cells.
[ii] i_{DCg} and I_g are the DC and fundamental current components, respectively.

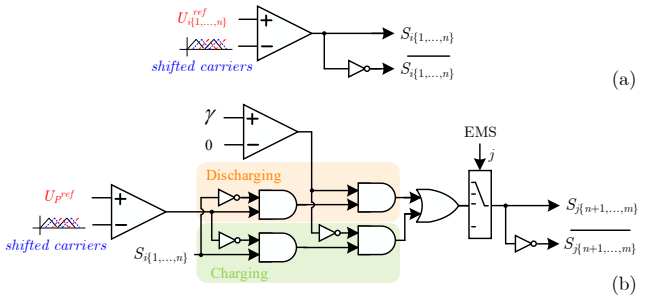

Fig. 4. Gating signals generation in the modified PS-PWM in (a) the PV cells; and (b) ES cells.

is inserted, as indicated by the orange color in Fig. 3(b). The PWM scheme used for the generation of such gating signals would be as sketched in Fig. 4. In this figure, the ES cells are assigned to the PV ones through a selector, which allows EMS interference and also having unequal ES cells to the PV ones. Note that, shifted triangular carriers were used here, on the consideration that the total number of cells is high, requiring a low switching frequency (f_s). The concept of employing shifted triangular carriers in low switching frequencies ensures a centered cells insertion. However, in case the total number of cells is relatively low, the efficiency of the system can be optimized by minimizing the switching loss using shifted sawtooth carriers. This pattern allows the ES cells to be inserted once per switching period (T_s) after the PV cells are inserted in both charging and discharging modes, instead of two times as is the case of using shifted triangular carriers.

To avoid an over-modulation case in the PV cells, at least one of the following can be resorted to:

1) Using the modified PS-PWM demonstrated earlier, which ensures that the voltage level at the output of the converter is not jeopardized during the charging mode with respect to the grid voltage.
2) Setting lower voltage in the ES cells v_{ES} than the voltage in the PV equivalents, expediting the power flow during the charging time interval within the switching cycle.
3) Injecting and absorbing the third harmonic component, within the converter, through the PV and ES, respectively, promoting higher power release from the PV cells to the ES ones during the first and last thirds of the grid half-cycles. This solution allows also mitigating the double-line-frequency (2ω) in the PV cell voltages provoked by the periodic instantaneous power delivery in the single-phase system.

D. Comparative study

The switching frequency, the current and voltage ratings, the power switches count, the inductors count, and the dead-band between the gate drive signals, in all the conventional CHB (Fig. 1(a) [12]), CHBB [14], and proposed topology are summarized in Table I. Note that, CHB-based topologies have been considered for comparison, as they share the same features with the proposed one from energy management perspective. Moreover, CHB structure is conventional and has been well investigated and utilized even by the industry. Comparing the switching frequency, it can be seen that, all cells in the CHB operate at f_s, while the CHBB operates at higher frequency than f_s on the PV boost stage side, considering design constraints of the inductors. In contrast, in the proposed topology there are some bridges, which operate at a switching frequency that is even less than f_s—the Sync-bridge operates at the line frequency f_g and the C/D-bridge at few seconds rate depending upon the weather conditions. Consequently, the switching loss should be less in the proposed topology. These loss will be calculated later according to the built prototype.

In term of current ratings, it can be seen that, the proposed topology is similar to its counterparts. Meanwhile, the voltage

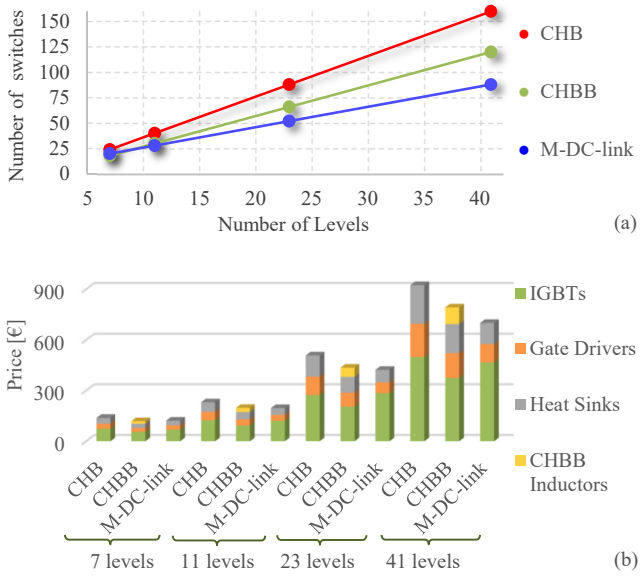

Fig. 5. PV-fed multilevel converters with integrated ES, in terms of (a) number of switches, and (b) element prices.

TABLE II.
GRID SPECIFICATIONS AND DESIGNED PARAMETERS OF BOTH THE MULTILEVEL DC-LINK CONVERTER WITH INTEGRATED ES AND CHB

f_g (Hz)	V_g (V)	I_g (A)	f_s (kHz)	L_f (mH)	v_{cell} (V)	C_{PV} (mF)	C_{ES} (mF)	L_b (mH)	n & m-n	IGBT[1]			
										CHB	Proposed topology		
											PV&ES cells	C/D-bridge	Sync-bridge
50	$230\sqrt{2}$	12	2.5	3.5	190	2	2	0.3	3	IRGP4072DPbF	IRGP4072DPbF	FGW35N60HC	FGW35N60HC

[1]Insulated-Gate Bipolar Transistor

ratings used in the proposed topology is higher in some power switches, such as those in the C/D- and Sync-bridges, since the voltage seen by these bridges is equal to the sum of the PV cells (or ES cells). The voltage stress is, however, similar in all three inverters. The underlying reason behind the voltage stress similarity despite the different voltage levels in the C/D- and Sync-bridges, is that the voltage change rate is according to one cell shaping the staircase output voltage waveform. As it can be seen from both Table I and Fig. 5(a), the proposed topology uses fewer power switches compared to the CHB and CHBB, especially in the high levels region since the eight switches in the C/D- and Sync-bridges become negligible. On the inductors side, they are employed only in the CHBB. One can see from the same table, that the Sync-bridge does not require dead-band between the gate drive signals since it inverts at the zero-voltage crossing point, where all cells are bypassed. Note that, the bidirectional-boost stages in the ES cells, as well as output filter are not considered in the comparative study along the paper since they are assumed to be equivalent from all aspects.

In order to have a realistic evaluation of the proposed topology in term of cost, averaged prices from several web stores of the aforementioned elements have been accounted. For the insulated-gate bipolar transistors (IGBT)s of the power cells, IRGP4072DPbF has been selected for all three converters in order to have a fair comparison. Due to the higher voltage ratings in the C/D- and Sync-bridges, FGW35N60HC, IKY40N120CS6, IXBH12N300, and IXYH30N450HV have been considered for the case of, respectively, 7, 11, 23, and 41 levels. The gate drivers and heat sinks have been chosen to be IR2102 and 625-45AB, respectively, for all power switches, while the boost inductors in the CHBB were SC-15-05JH model. As it can be seen from Fig. 5(b), which shows the resulted prices, although the proposed converter employs fewer IGBTs, their price is still almost similar to the CHB's and CHBB's, for all considered levels. This is mainly due to the higher price of the C/D- and Sync-bridge switches, as their voltage ratings increase with the levels increase. Nevertheless, the proposal is cheaper than the CHB since it still employs fewer gate drivers and heat sinks. The CHBB employs fewer IGBTs than the CHB, it is, therefore, cheaper. However, the CHBB is still more expensive than the proposal due to the employed inductors.

IV. SIMULATION RESULTS

A. System Description

For the sake of the experimental validation of the operation, analysis, and modulation of the proposed topology, a reduced scale 2-kW system has been designed, where its specifications and designed parameters are shown in Table II. The design constraints were an inductor peak-to-peak current ripple of 25% in the bidirectional-boost stage of the ES cells, and a capacitor peak-to-peak voltage ripple of 5% in both the PV and ES cells.

TABLE III.
PV MODULES AND BATTERIES CHARACTERISTICS

PV Parameter	Value	Battery Parameter	Value
Current at MPP, i_{MPP}	4A	Cell nominal voltage, v_{bat}	3.6V
Voltage at MPP, v_{MPP}	30V	Cell rated capacity, Q	2.6Ah

The PV modules were ASS 120 W-60/125m model from Automotive Solar Systems GmbH, and the key characteristics that were taken from their datasheet are listed in Table III. In order to achieve the required voltage level for grid-connection, five PV modules were connected in series in each PV cell. The battery packs were assembled by three strings, ten cells in each, using lithium-ion type cells, referenced as ICR18650, whose specifications are listed in Table III too. For testing the proposed topology, the control structure reported in [5], has been employed here, where minor changes including EMS and modulation have been introduced since the referred controller is for PV-fed CHB without ES.

B. Tests

Since the proposed converter is prone to different operating scenarios, it has been tested accordingly. The system is tested in three seconds test, where in each second, the irradiance changes, emulating different operating conditions. Fig. 6. shows the whole test, where the harvested PV powers, PV

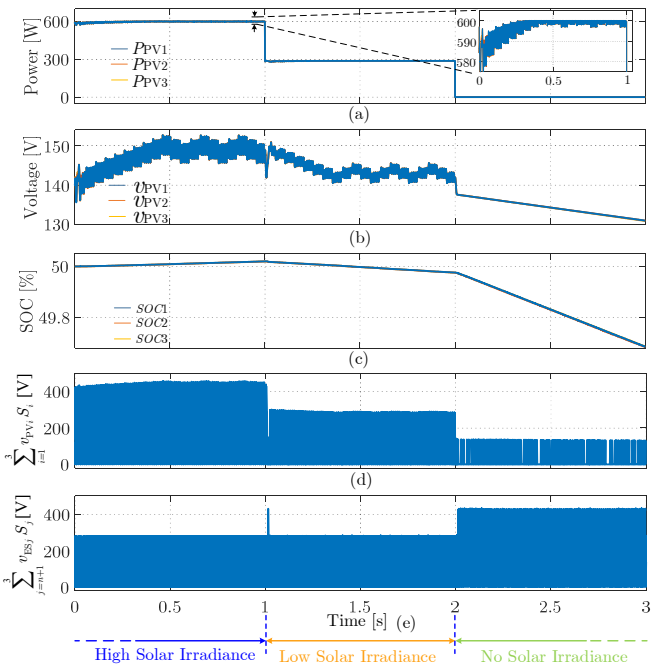

Fig. 6. The simulation test performed on the proposed topology, consisting of different weather conditions.

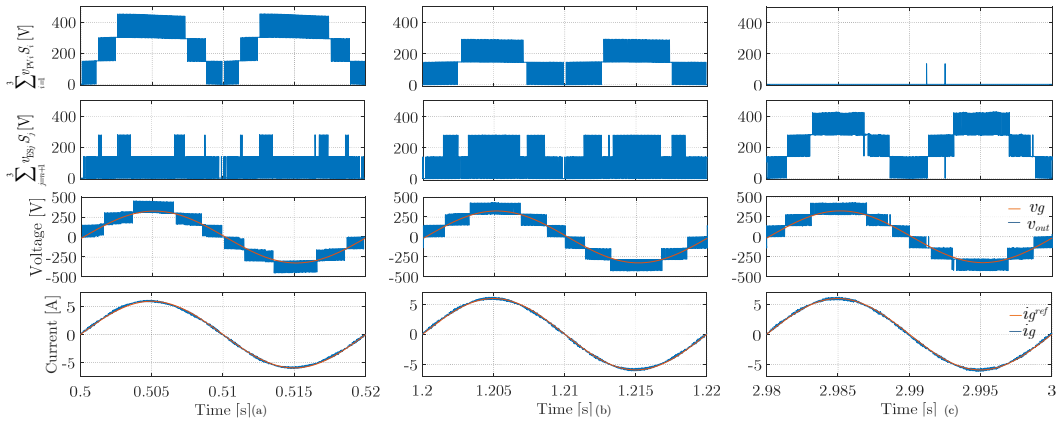

Fig. 7. A zoomed view on the sum of the output voltages at the PV and ES cells, in addition to the converter's output voltage and current: (a) high solar irradiance; (b) medium solar irradiance; and (c) a complete absence of the solar irradiance.

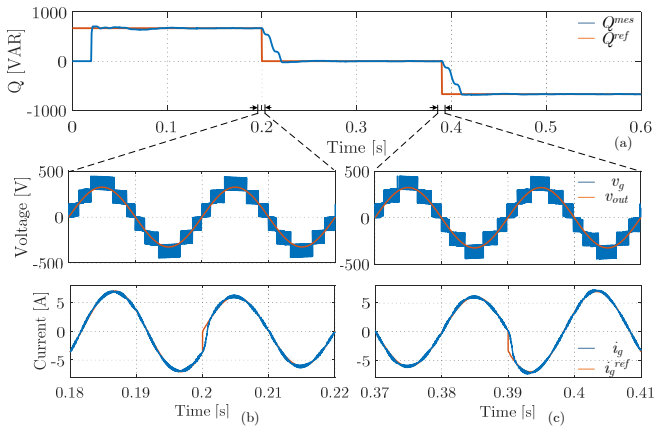

Fig. 8. The M-DC-link's output voltage and current in case of reactive power changes.

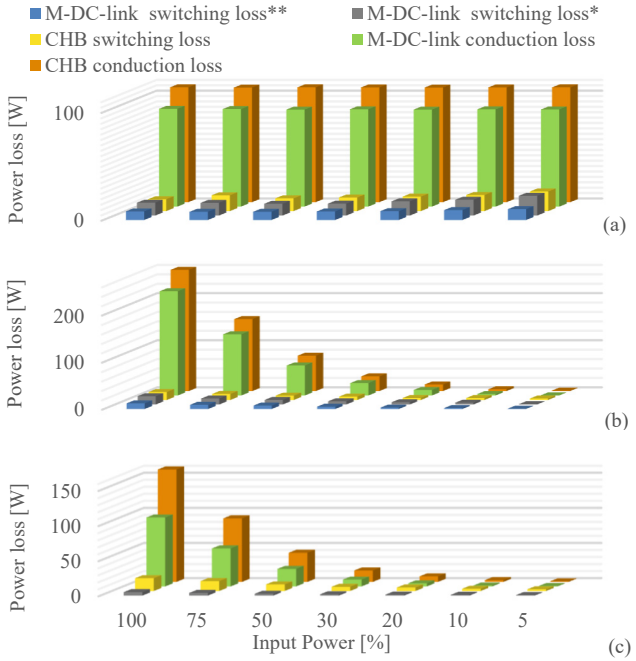

Fig. 9. Switching and conduction loss of both the proposed M-DC-link topology and CHB under (a) the European efficiency test, (b) modified European efficiency test, and (c) European efficiency test when the batteries float. * Shifted triangular carrier. ** Shifted sawtooth carrier.

The first time-interval of the test is when the PV panels are subjected to high solar irradiance, where the harvested power is higher than the power planned to be injected to the grid, which is in the three test time-intervals assumed to be 1kW. Since the period of the sum of the output voltages of the PV cells, as well as of the ES cells is smaller than the whole test duration, they are shown in enlarged form in Fig. 7(a). The output voltage of the converter, the grid voltage, and the current injected to the grid are also shown in the same figure. As it can be seen from the grid current in Fig. 7(a), the proposed converter is prosperously injecting a current that is conforming to its given reference, although the extracted PV power is higher. Meanwhile, from both Fig. 6(c), and ES cells voltage shown in Fig. 7(a), the batteries are absorbing the surplus of power through the negative voltage applied to them using the C/D-bridge, while maintaining the staircase output voltage waveform.

In the second time-interval, the solar irradiance decreases to 500W/m^2 among all PV cells, emulating a cloudy period in the day. According to the PV modules datasheet, under this irradiance level the PV panels generate lower power than the one planned to be injected to the grid, which is consistent with the obtained results in Fig. 6 (a). Similar to the first time-interval, a zoomed view of the second one is shown in Fig. 7(b). One can see from the grid current in Fig. 7(b) that, although the generated power from the PV arrays is less than the required one, the proposed converter is still injecting a current to the grid according to its provided reference through the energy stored in the batteries. As it can be observed from Fig. 6(c) and Fig. 7(b), the batteries are injecting the deficit of power through the positive voltage applied by the C/D-bridge, while the staircase output voltage waveform is retained.

In the third time-interval, the PV cells operate under a complete absence of the solar irradiance, emulating night times. As it can be seen from Fig. 6(a), the PV powers is nulled, while as shown in Fig. 6(b), the PV cells preserved a voltage above 130V in the capacitors, each, which is due to the minimum duty cycle provided by the control algorithm, on the account to rise the voltage back to its reference.

It is worth to shed the light on the width of the converters' output voltage at the last level in both positive and negative grid half-cycles in Fig. 7(a), (b), and (c). The reason that the voltage width in the last level in Fig. 7(b) and (c) is larger than in Fig. 7(a) lies on the fact the voltage amplitude in Fig. 7(a) is higher due to the high solar irradiance.

Another test has been performed considering that both the solar irradiance and output active power are fixed, while the reactive power (Q) changes from 650 to 0VAR, and then from 0 to -650VAR. As it can be seen from Fig. 8, which shows the corresponding results, the proposed inverter is confirming its capability for reactive power exchange, as it is well injecting and absorbing it according to its given reference.

C. Efficiency

Finally, the switching and conduction loss in both the CHB and proposed M-DC-link converter with built-in ES are calculated using PLECS toolbox based on the devices real datasheets, which are corresponding to the models stated in subsection III.D. Note that, for accessing the switching and conduction loss, the modified PS-PWM has been applied on both the proposed and CHB topologies.

Fig. 9(a) shows the calculated loss for these converters when they were operating under the European efficiency (η_{Euro}) test, where the power injected to the grid was kept at 1kW for all irradiance levels. The European efficiency is assessed as,

$$\begin{aligned}\eta_{\mathrm{Euro}} = {} & 0.2\eta_{100\%} + 0.48\eta_{50\%} + 0.1\eta_{30\%} \\ & + 0.13\eta_{20\%} + 0.06\eta_{10\%} + 0.03\eta_{5\%}\end{aligned} \tag{11}$$

such as, $\eta_{100\%}$ stands for the efficiency of the converter operating under 100% of the solar irradiance of the standard test conditions (STC). As it can be seen from this figure, the proposed topology suffers from less conduction loss, while the switching loss are also less but the improvement is insignificant. The differences in the conduction loss are important since in the proposed converter the line current crosses one switch in each cell, in addition to the two switches of the C/D- and Sync-bridges at every instant, while in the CHB topology it crosses two switches in each cell. The European efficiency of the proposed topology and CHB were measured as 96.06% and 95.41%, respectively. The switching loss are further minimized through the shifted sawtooth carriers, as shown in blue color in the same figure, improving the efficiency up to 96.2%.

The European efficiency test, however, considers the change in the power level on the PV side only, restricting the test of PV-fed converters with integrated ES to one operating point according to the power injected to the grid as confirmed by the displayed power loss in Fig. 9(a). A modified efficiency evaluation test is, therefore, introduced in this paper, allowing the PV-fed converters with built-in ES to be tested under the whole power operating range according to the following formula,

$$\begin{aligned}\eta_{\mathrm{MEuro}}^{\mathrm{ES}} = {} & 0.2\eta_{100\%}^{30\%} + 0.48\eta_{50\%}^{20\%} + 0.1\eta_{30\%}^{15\%} \\ & + 0.13\eta_{20\%}^{10\%} + 0.06\eta_{10\%}^{5\%} + 0.03\eta_{5\%}^{0\%}.\end{aligned} \tag{12}$$

where the subscripts still follow the same definition as in the European efficiency, while superscripts correspond to the power drawn from ES cells. Therefore, $\eta_{100\%}^{30\%}$ denotes to PV arrays subjected to $1000\mathrm{W/m^2}$ solar irradiance and the batteries are injecting 30% of this power. According to this analysis, the converter should be designed for higher power than the adopted PV power rating in order to inject power from the batteries even if the PV arrays are producing their maximum power, if needed. The case of $\eta_{100\%}^{30\%}$ has been specifically added into the efficiency evaluation test to emulate the situation when the converter contributes to grid ancillary services, such as voltage support and frequency regulation (e.g. to cope with external disturbances). The modified European efficiency for the evaluation of both the proposed topology and CHB were measured as 96.44% and 95.85%, respectively, and their detailed switching and conduction loss are displayed in Fig. 9(b). The efficiency can be again further improved by reducing the switching loss through the shifted sawtooth carriers up to 96.58%.

Another test was done considering the case where the batteries float, i.e. simulating the system under one of the following cases:

1) The power injected to the grid just equals the power drawn from the PV panels;
2) The power that needs to be injected to the grid is higher than the one harvested, but the batteries SOCs reached their minimum; or
3) The power that needs to be injected to the grid is less than the one harvested, but the batteries SOCs reached their maximum. The latter case happens more often since the batteries' SOC usually reach SOC_{max} around noon.

The European efficiency of both the proposed topology and CHB were measured as 98.13% and 96.55%, respectively, while their detailed switching and conduction loss are shown in Fig. 9(c). It is noteworthy from the registered efficiencies and Fig. 9(c) that, the difference between the two converters during this test is significant. The underlying reason behind the prominent efficiency of the proposed converter in this test is that, the ES cells can be bypassed using the C/D-bridge when they are in float mode, opposed to the CHB's case where the line current flows through all cells even if they are neither injecting power nor absorbing it.

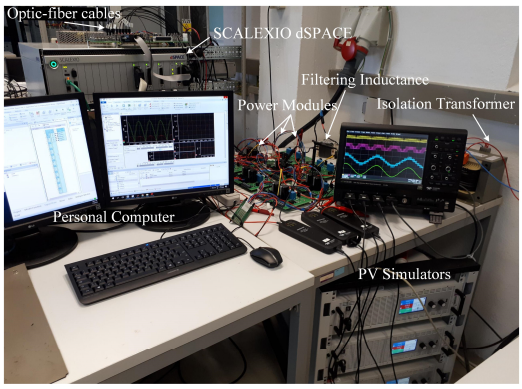

Fig. 10. The built experimental test bench for validating the proposed topology.

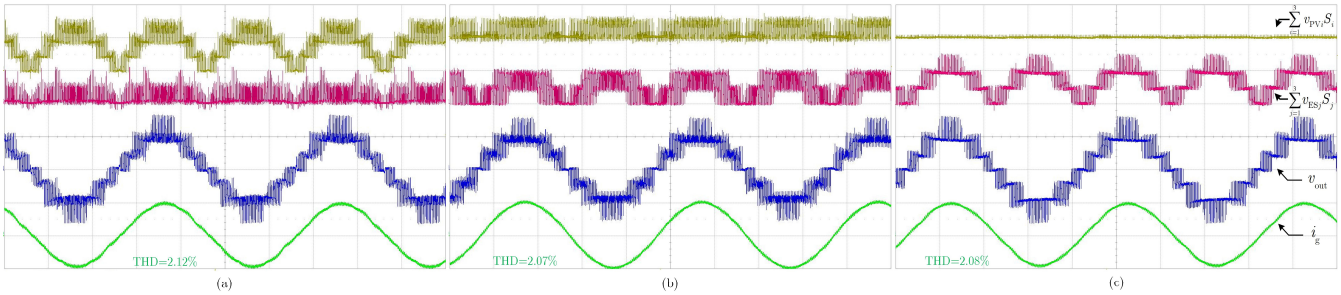

Fig. 11. The experimental results of the proposed topology during: (a) high solar irradiance; (b) medium solar irradiance; and (c) a complete absence of the solar irradiance (300V/Div for the voltages, 3A/Div for the current, and 5ms/Div for the time).

V. Experimental Validation

According to the specifications given in the simulation section, a real prototype has been built to experimentally validate the operation, analysis, and modulation of the proposed converter (see Tables II and III). The power modules were custom made. For testing the PV panels with flexibility in changing the solar irradiance, three PV emulators from Electro-Automatic, model PSI 91500-30, have been used. For emulating the batteries, they have been replaced by Chroma programmable electronic loads, model 638004, during the charging mode, and replaced by Intepro DC-sources, model PS9000, during the discharging one. For running the control algorithm, SCALEXIO from dSPACE has been used. The used SCALEXIO have one DS6001 processing board, two DS2655M2 field programmable gate arrays (FPGA), and three DS6221 analogue to digital conversion (A/D) boards. The developed modulation strategy, which is presented in section III, has been programmed on one of the DS2655M2 FPGAs, with a resolution of 9ns. The control algorithm has been implemented on the DS6001 processing board, which sends the command signals to the DS2655M2 FPGA with an update rate according to the switching frequency. The DS6001 processing board receives the analogue measured signals converted to digital through the DS6221 A/D conversion board.

Similarly to the simulations, the system has been tested in the experiment. The system started operating under high solar irradiance, generating power higher than the power reference. The sum of the output voltages of the PV cells, the sum of the output voltages of the ES cells, the converter output voltage, and the current injected to the grid, during this mode of operation are shown in Fig. 11(a). As it can be seen from this figure, the PVs' output voltage is higher than the converter's output voltage. One can see from the current injected to the grid that it is conforming to the current reference, where the excess of power is distributed to the ES cells.

Secondly, the solar irradiance has been decreased in the PV emulators so that the generated power is lower than the inquired active power. The sum of the output voltages of the PV cells, the sum of the output voltages of the ES cells, the converter's output voltage, and the current injected to the grid, during this operating mode are shown in Fig. 11(b). As it can be seen from this figure, although the PV cell voltages are low, the current injected to the grid is at the same level of its reference, where the ES cells are compensating for the lack of power.

Lastly, the power from the PV simulators was stopped, emulating PV arrays during night times. The sum of the output voltages of the PV cells, the sum of the output voltages of the ES cells, the converter's output voltage, and the current injected to the grid, during this test condition are shown in Fig. 11(c). As one can see from this figure, the ES cells are successfully injecting current to the grid in agreement with the inquired active power; despite the complete absence of the PV arrays.

Note that, in all performed tests the proposed converter has retained the step-like output voltage, promoting the use of a smaller output filter, as well as evading the over-modulation issue, which exists in most PV+ES multilevel converters. The maximum total harmonic distortion (THD) has been calculated as 2.12%, which is corresponding to the charging mode; however, the difference is insignificant compared to those of the remaining modes.

VI. Conclusion

This paper proposed a M-DC-link converter, along with a modified PS-PWM for PV systems with built-in ES. The proposal performance was examined based on two different carrier signals, namely; the shifted triangular carrier and shifted sawtooth carrier. Moreover, the proposed M-DC-link converter with integrated ES was compared to the classical CHB-based architectures in terms of semiconductor devices' count and switching frequency, voltage ratings and stress, current ratings, and more importantly cost.

The proposed topology offers the same advantages of the CHB equivalent, as well as the following further advantages:

1) lower switch-count, which could reach around 50% when using high cells' count;
2) lower conduction loss. In addition, the conduction loss are further improved during batteries float mode since the ES cells can be bypassed using the C/D-bridge;
3) lower switching frequency in some switches, yielding into lower switching loss;

On the other hand, it suffers from higher voltage ratings in the employed C/D- and Sync-bridge switches.

Finally, the proposed converter has been experimentally tested under different weather conditions to cover several possible scenarios, where it was shown that the proposal is feasible and multifunctional.

VII. REFERENCES

[1] V. Sonti, S. Jain and S. Bhattacharya, "Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156-1169, Feb. 2017.

[2] Y. Yu, G. Konstantinou, C. D. Townsend, R. P. Aguilera and V. G. Agelidis, "Delta-Connected Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Grid Integration," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8877-8886, Nov. 2017.

[3] Liming Liu et al, "Decoupled Active and Reactive Power Control for Large-Scale Grid-Connected Photovoltaic Systems Using Cascaded Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol.30, no.1, pp.176-187, Jan. 2015.

[4] F. Rong, X. Gong, and S. Huang, "A Novel Grid-Connected PV System Based on MMC to Get the Maximum Power under Partial Shading Conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4320–4333, 2017.

[5] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, 2009.

[6] Y. Fayyad and L. Ben-Brahim, "Multilevel cascaded Z source inverter for PV power generation system," *Int. Conf. on Renewable Energy Research and Applications*, Nagasaki, 2012, pp. 1-6.

[7] Y. Liu, B. Ge, H. Abu-Rub and F. Z. Peng, "An Effective Control Method for Three-Phase Quasi-Z-Source Cascaded Multilevel Inverter Based Grid-Tie Photovoltaic Power System," *IEEE Trans. Ind. Electron*, vol. 61, no. 12, pp. 6794-6802, Dec. 2014.

[8] I. Abdalla, J. Corda, and L. Zhang, "Multilevel DC-link inverter and control algorithm to overcome the PV partial shading," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 14–18, 2013.

[9] R. Uthirasamy, V. Kumar Chinnaiyan, U. S. Ragupathy, and J. Karpagam, "Investigation on three-phase seven-level cascaded DC-link converter using carrier level shifted modulation schemes for solar PV system applications," *IET Renew. Power Gener.*, vol. 12, no. 4, pp. 439–449, 2018.

[10] W. Yuan, J. Yang, Y. Sun, H. Han, X. Hou and M. Su, "A novel operation mode for PV-storage independent microgrids with MPPT based droop control," *IEEE 3rd Int. Future Energy Electronics Conf. and ECCE Asia,* Kaohsiung, 2017, pp. 936-941.

[11] N. Saxena, I. Hussain, B. Singh, and A. L. Vyas, "Implementation of Grid Integrated PV-Battery System for Residential and Electrical Vehicle Applications," *IEEE Trans. Ind. Electron.*, vol. 46, no. c, 2017.

[12] Qinghao Zhang, "Control of PV battery hybrid system using Cascaded H Bridge converter," *IEEE 3rd Int. Future Energy Electronics Conf. and ECCE Asia, Kaohsiung*, 2017, pp. 2008-2012.

[13] L. Xiong, Y. Gui, H. Liu, W. Yang and J. Gong, "A hybrid CHB multilevel inverter with supercapacitor energy storage for grid-connected photovoltaic systems," *IEEE Applied Power Electronics Conf. and Exposition*, San Antonio, TX, 2018, pp. 3195-3199.

[14] V. Verma and A. Kumar, "Power balanced cascaded multilevel inverter fed scalar controlled induction motor pump sourced from photovoltaic source," *IEEE Int. Conf. on Power Electronics, Drives and Energy Systems* (PEDES), Bengaluru, 2012, pp. 1-6.

[15] A. Marquez, J. I. Leon, S. Vazquez, L. G. Franquelo and S. Kouro, "Operation of an hybrid PV-battery system with improved harmonic performance," *43rd Annual Conf. of the IEEE Industrial Electronics Society*, Beijing, 2017, pp. 4272-4277.

[16] S. Vavilapalli, U. Subramaniam, S. Padmanaban and V. K. Ramachandaramurthy, "Design and Real-Time Simulation of an AC Voltage Regulator Based Battery Charger for Large-Scale PV-Grid Energy Storage Systems," *IEEE Access*, vol. 5, pp. 25158-25170, 2017.

[17] H. Nademi, Z. Soghomonian and L. Norum, "A robust predictive MPPT strategy: An enabler for improving the photovoltaic conversion source," *IEEE 6th Int. Conf. on Renewable Energy Research and Applications,* San Diego, CA, 2017, pp. 1086-1091.

[18] B. Ge et al., "An Energy-Stored Quasi-Z-Source Inverter for Application to Photovoltaic Power System," *IEEE Trans. Ind. Electron*., vol. 60, no. 10, pp. 4468-4481, Oct. 2013.

[19] J. G. Cintron, Y. Li, S. Jiang, and F. Z. Peng, "Quasi-Z-source inverter with energy storage for photovoltaic power generation systems*," Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo*., Mar. 2011, pp. 401–406.

[20] D. Sun, B. Ge, W. Liang, H. Abu-Rub and F. Z. Peng, "An Energy Stored Quasi-Z-Source Cascade Multilevel Inverter-Based Photovoltaic Power Generation System," *IEEE Trans. Ind. Electron*, vol. 62, no. 9, pp. 5458-5467, Sept. 2015.

[21] A. Lashab, D. Sera, J. Martins and J. M. Guerrero, "Multilevel DC-Link Converter-Based Photovoltaic System with Integrated Energy Storage," *5th Int. Symp. Environment-Friendly Energies App. (EFEA)*, Rome, 2018, pp. 1-6.

[22] H. Jafarian, N. Kim and B. Parkhideh, "Decentralized Control Strategy for AC-Stacked PV Inverter Architecture Under Grid Background Harmonics," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 84-93, March 2018.

[23] H. Jafarian, S. Bhowmik and B. Parkhideh, "Hybrid Current-/Voltage-Mode Control Scheme for Distributed AC-Stacked PV Inverter With Low-Bandwidth Communication Requirements," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 321-330, Jan. 2018.

[24] Q. Zhang and K. Sun, "A Flexible Power Control for PV-Battery-Hybrid System Using Cascaded H-Bridge Converters," *IEEE J. Emerg. Sel. Top. Power Electron.*, Accepted, 2018.

[25] Y. Zhou, L. Liu, H. Li and L. Wang, "Real time digital simulation (RTDS) of a novel battery-integrated PV system for high penetration application," *2nd Int. Sympo. Power Electron. Distributed Generation Systems,* Hefei, 2010, pp. 786-790.

Abderezak Lashab (S'13) received the baccalaureate in 2007 with "honor", ranked as the First in the high school Cheikh Ibrahim Bayoud, Constantine, Algeria. He received the bachelor's and master's degrees in electrical engineering in 2010 and 2012, respectively, from Université des Frères Mentouri Constantine 1, Constantine, Algeria. He is currently working toward the Ph.D. degree on developing and investigating new converter topologies and control methods of photovoltaic systems with and without storage with the Department of Energy Technology, Aalborg University, Denmark.

From the year 2013 to 2014, he served as an engineer in High Tech Systems (HTS). From 2014 to 2016, he was a Lecturer Assistant in the Université des Frères Mentouri Constantine 1, where he helped in teaching several electrical engineering courses for undergraduate students. He was a Visiting Researcher at the Chair of Power Electronics, Kiel University, Germany from April to July 2019. His current research interests include power electronics topologies, modeling, and control for photovoltaic systems with and without storage.

He also serves as a Reviewer in the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS, IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, IET Power Electronics, IET Electronics Letters, and several IEEE conferences.

Dezso Sera (S'05–M'08–SM'15) received the B.Sc. and M.Sc. degrees in electrical engineering from the Technical University of Cluj, Cluj-Napoca, Romania, in 2001 and 2002, respectively, the M.Sc. degree in power electronics and the Ph.D. degree in PV systems from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, where he is currently an Associate Professor. Since 2009, he has been a Leader of the Photovoltaic Systems Research Program (www.pv-systems.et.aau.dk) at the same department.

His research interests include modeling, characterization, diagnostics and maximum power point tracking (MPPT) of PV arrays, as well as power electronics, and grid integration for PV systems.

Frederik Hahn (S'16) received the bachelor's and master's degrees in electrical engineering from Christian-Albrechts-University of Kiel (CAU), Kiel, Germany in 2013 and 2015, respectively. His master's thesis took place in collaboration with Siemens AG, Erlangen, Germany. Since 2015 he has been working toward the Ph.D. degree with the Chair of Power Electronics, CAU. In 2017, he was a visiting researcher at Aalborg University, Aalborg, Denmark. His current research interests include modular power converters for renewable high-power applications and reliability in power electronics.

Luis Juarez Camurca received his B.S. degree in electrical engineering from the Federal University of Ceará, Fortaleza, Brazil, in 2012 and obtained his M.S. degree from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2016. He is currently working towards his Ph.D. degreee at the Chair of Power Electronics, Kiel University, Kiel, Germany. His research interests include dc-ac converters, multilevel topologies and wide-badgap semiconductors.

Marco Liserre (S'00-M'02-SM'07-F'13) received the MSc and PhD degree in Electrical Engineering from the Bari Polytechnic, respectively in 1998 and 2002. He has been Associate Professor at Bari Polytechnic and from 2012 Professor in reliable power electronics at Aalborg University (Denmark). From 2013 he is Full Professor and he holds the Chair of Power Electronics at Kiel University (Germany). He has published 400 technical papers (more than 1/3 of them in international peer-reviewed journals) and a book. These works have received more than 28000 citations. Marco Liserre is listed in ISI Thomson report "The world's most influential scientific minds" from 2014.

He has been awarded with an ERC Consolidator Grant for the project "The Highly Efficient And Reliable smart Transformer (HEART), a new Heart for the Electric Distribution System".

He is member of IAS, PELS, PES and IES. He has been serving all these societies in different capacities. He has received the IES 2009 Early Career Award, the IES 2011 Anthony J. Hornfeck Service Award, the 2014 Dr. Bimal Bose Energy Systems Award, the 2011 Industrial Electronics Magazine best paper award and the Third Prize paper award by the Industrial Power Converter Committee at ECCE 2012, 2012, 2017 IEEE PELS Sustainable Energy Systems Technical Achievement Award and the 2018 IEEE-IES Mittelmann Achievement Award.

Josep M. Guerrero (S'01-M'04-SM'08-FM'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program (www.microgrids.et.aau.dk). From 2014 he is chair Professor in Shandong University; from 2015 he is a distinguished guest Professor in Hunan University; and from 2016 he is a visiting professor fellow at Aston University, UK, and a guest Professor at the Nanjing University of Posts and Telecommunications. From 2019, he became a Villum Investigator by The Villum Fonden, which supports the Centre for Research on Microgrids (CROM) at Aalborg University, being Prof. Guerrero the founder and Director of the same centre.

His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering and the internet of things for AC/DC microgrid clusters and islanded minigrids. Specially focused on maritime microgrids for electrical ships, vessels, ferries and seaports. Prof. Guerrero is an Associate Editor for a number of IEEE TRANSACTIONS. He has published more than 500 journal papers in the fields of microgrids and renewable energy systems, which are cited more than 40,000 times. He received the best paper award of the IEEE Transactions on Energy Conversion for the period 2014-2015, and the best paper prize of IEEE-PES in 2015. As well, he received the best paper award of the Journal of Power Electronics in 2016. During six consecutive years, from 2014 to 2019, he was awarded by Clarivate Analytics (former Thomson Reuters) as Highly Cited Researcher. In 2015 he was elevated as IEEE Fellow for his contributions on "distributed power systems and microgrids."